41th IEEE International Symposium on Multiple-Valued Logic
ISMVL 2011

May 23-25, 2011, Tuusula, Finland.

CALL FOR PAPERS

The Multiple-Valued Logic Technical Committee of the IEEE Computer Society will hold its 41th annual symposium on May 23-25, 2011, in Tuusula, Finland.

- Algebra and Formal Aspects
- ATPG and SAT
- Automatic Reasoning
- Circuit/Device Implementation
- Communication Systems
- Computer Arithmetic
- Data Mining
- Fuzzy Systems and Soft Computing
- Image Processing
- Logic Design and Switching Theory
- Logic Programming
- Machine Learning and Robotics
- Mathematical Fuzzy Logic
- Nano-Technology
- Philosophical Aspects
- Quantum Computing
- Signal Processing
- Spectral Techniques
- Verification

Authors should submit papers by November 1, 2010 using the software that will be available on the conference web site. Each manuscript should include a 50-100 word abstract, and should not exceed 6 pages in the 2-column IEEE Proceedings format.

A selection of the papers presented at the ISMVL 2011 will be invited to provide an extended version to be published in a special issue of the *Journal of Multiple-Valued Logic and Soft Computing.*

Tentative Dates:
November 1, 2010 Paper submission,
February 1, 2011 Author notification,
March 1, 2011 Final version,
April 10, 2011 Early registration deadline,
May 23-25, 2011 ISMVL 2011 Symposium.

TICSP Tampere International Center for Signal Processing
TAMPERE UNIVERSITY OF TECHNOLOGY